

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**

What is claimed is:

1. Semiconductor structure, comprising:

5 a buried first semiconductor layer of a first doping type;

a second semiconductor layer of the first doping type on the buried semiconductor layer, which is less doped than the buried first semiconductor layer;

10

a semiconductor area of a second doping type on the second semiconductor layer, so that a pn junction is formed between the semiconductor area and the second semiconductor layer; and

15

a recess present below the semiconductor area in the buried first semiconductor layer, which contains a semiconductor material of the first doping type, which lies deeper in the substrate than the buried first semiconductor layer, such  
20 that the breakdown voltage across the pn junction is higher than if the recess were not provided.

2. Semiconductor structure according to claim 1, wherein the second semiconductor layer extends into the recess and  
25 the recess further has another semiconductor area of the first doping type, which is heavier doped than the second semiconductor layer.

3. Semiconductor structure according to claim 2, wherein  
30 the further semiconductor area is doped equal or less than the buried first semiconductor layer.

4. Semiconductor structure according to claim 1, wherein the recess fully penetrates the buried first semiconductor  
35 layer.

5. Semiconductor structure according to claim 1, wherein the semiconductor area is a base, the first buried

200250232

24

semiconductor layer a subcollector and the second semiconductor layer a collector of a bipolar transistor.

5 6. Semiconductor structure according to claim 5, wherein the buried first semiconductor layer further represents a subcollector for at least another bipolar transistor, wherein the buried first semiconductor layer has no or such recess for at least another bipolar transistor, that the bipolar transistors have different breakdown voltages.

10 7. Semiconductor structure according to claim 6, wherein the buried first semiconductor layer has recesses of different widths for the bipolar transistors.

15 8. Method for providing a semiconductor structure according claim 1, further comprising:

providing the buried first semiconductor layer with the recess formed therein;

20 generating the further semiconductor area in the recess;

25 introducing the semiconductor material of the first doping type into the recess, wherein after the step of introducing the semiconductor material lies deeper in the substrate than the buried first semiconductor layer;

30 generating the second semiconductor layer on the buried first semiconductor layer, which is less doped than the buried first semiconductor layer;

generating the semiconductor area on the second semiconductor layer.

35 9. Method according to claim 8, wherein the step of providing comprises:

depositing an implantation mask on a semiconductor substrate, wherein the implantation mask covers the recess;

5 implanting the buried first semiconductor layer by using the implantation mask.

10. Method according to claim 8, further comprising:

10 depositing a further implantation mask, which leaves a recess exposed, after the step of providing;

generating a further semiconductor area in the recess by using the further implantation mask.

15 11. Method according to claim 8, further comprising:

depositing a further implantation mask, which leaves the recess exposed, after the step of generating the second semiconductor layer and

20

generating a further semiconductor area in the recess by using the further implantation mask.